REMARKS

This application has been carefully reviewed in light of the Office Action dated June 3, 2004. Applicant has amended claims 10-12. Reconsideration and favorable action in this case are respectfully requested.

The Examiner has rejected claims 1, 4-6, 8, 10, 11, 13, 14 and 17-19 under 35 U.S.C. §102(b) as being unpatentable over U.S. Pat. No. 6,161,162 to DeRoo. Applicants have reviewed this reference in detail and do not believe that it discloses or makes obvious the invention as claimed.

The Examiner has rejected claims 2, 3, 7, 9, 12, 15, 16 and 20 under 35 U.S.C. §103(a) as being unpatentable over DeRoo in view of U.S. Pat. No. 5,887,146 to Baxter. Applicants have reviewed these references in detail and do not believe that they disclose or make obvious the invention as claimed.

Claims 10-12 have been amended to properly identify the claims as method claims.

The DeRoo reference is directed to a multiprocessing computer system with multiplexed address and data paths from multiple CPUs to a single storage device. The paths to the storage device are controlled by an arbitration circuit that allows one CPU to always have the highest priority.

The DeRoo reference is completely different from the invention claimed in independent claim 1. Claim 1 recites the following elements:

> a master processor;
>
> a system memory;
>
> a slave processor subsystem including:
>
> a slave processor;
>
> a shared memory accessible by said master processor and said slave processor; and

an external memory interface allowing said slave processor to access said system memory; and

a verification interface for passing system memory accesses to said system memory in a normal mode and for passing said system memory accesses to said shared memory in a verification mode.

Importantly, the "verification interface for passing system memory accesses to the system memory in a normal mode and for passing the system memory accesses to the shared memory in a verification mode" is not shown in the DeRoo reference.

The Examiner cites column 81, line 50 through column 82, line 6, as showing the verification interface. The citation by the Examiner is as follows:

> Full access is provided to both the CPU 702, as well as the SCP 706, utilizing a time based interleaving method as illustrated in FIG. 24 and described in more detail below. In this method, the SCP 706 normally has priority to the common memory device 704 in a shared mode of operation. In order for the SCP 706 to gain exclusive control, the CPU 702 may be forced into a wait state by the HUI 700 by pulling the input/output channel ready signal IOCHRDY inactive. In particular, exclusive use of the common memory device 704 can be given to the SCP 706 by asserting a CPU EXCLUDED signal by way of the SCP 706 control of a Flash Memory register, FLASH_GRAB, at address 43H in the SCP register file 714; read by the CPU 702 as bit 1 of a flash interface control register FLASH_CTRL; read-only by the CPU 702. During conditions when the SCP has exclusive access of the common memory device 704, the CPU 702 can gain control by forcing the SCP 706 into reset by setting bit 0 of the flash interface control register FLASH_CTRL. Alternatively, the CPU 702 can gain exclusive control of the common memory device 704 by placing the SCP 706 into a reset state by setting bit 0 of the flash interface control register FLASH_CTRL. In a shared mode, bits 0 and 1 of the flash interface control register FLASH_CTRL are deasserted.

This passage only indicates that the CPU 702 and SCP 706 can both access the common memory device 704, normally in a shared mode of operation, but either can gain exclusive control. The SCP can gain exclusive control by asserting a CPU EXCLUDED and the CPU can gain exclusive control by resetting SCP 706.

DeRoo does not show a verification interface where memory accesses are directed to a first memory (system memory) in a normal mode and to a second memory (shared memory in the slave processor subsystem) in a verification mode. DeRoo does not discuss a normal mode and a verification mode, nor does DeRoo discuss circuitry providing access to different memories responsive to different modes.

The DeRoo reference would not be able to provide the debugging capabilities of the present invention, because it does not have the capability to selectively re-direct memory access requests intended for the system memory to a shared memory in the slave processor subsystem while in a verification mode. Thus, in verification mode, the slave processor subsystem can be completely isolated from the master processor subsystem. This is not true of DeRoo.

Accordingly, Applicants believe that claim 1 is allowable over the DeRoo reference. Additionally, Applicants believe dependent claims 2 through 7 are allowable as well.

For the reasons stated above, Applicant believes that method claims 8-12 are allowable as well.

Further, for the reasons stated above, Applicant believes that claims 13-20 are allowable as well.

An extension of one month is requested and a Request for Extension of Time under § 1.136 with the appropriate fee is attached hereto.

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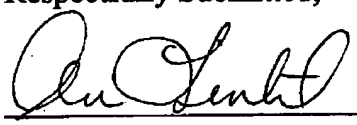
The Commissioner is hereby authorized to charge any fees or credit any overpayment, including extension fees, to Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Alan W. Lintel, Applicants' Attorney at (972) 664-9595 so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,



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